In the Claims:

Please amend claims 1 and 9 as follows:

1. (Currently Amended) A ~~pseudo-NMOS~~ logic circuit comprising:

a pseudo-NMOS circuit, said pseudo-NMOS circuit comprising:

a first PFET electrically connected between a power supply and an output node;

an NFET circuit connected between said output node and ground and having a plurality of inputs;

a second PFET electrically connected between said power supply and said output node, said second PFET being controlled by a signal at said output node;

a control circuit for turning said second PFET ON and OFF based on said signal at said output node;

wherein said control circuit sets said second PFET to ON when said signal at said output node is HIGH, and sets said second PFET to OFF when said signal at said output node is LOW.

2. (Cancelled)

3. (Previously Presented) The circuit as defined in claim 1 wherein said control circuit is electrically connected between said power supply and said ground, and has an input connected to said output node.

4. (Original) The circuit as defined in claim 3 wherein said control circuit is an inverter circuit including a PFET connected in series to an NFET, and wherein said PFET is electrically connected to said power supply, said NFET is connected to said ground, and gates of said PFET and NFET are connected to said output node.

5. (Original) The circuit as defined in claim 4 wherein a gate to said second PFET is connected to a feedback node connecting a drain of said PFET and a drain of said NFET of said inverter circuit.

6. (Original) The circuit as defined in claim 5 wherein a signal at said feedback node transitions LOW to turn ON said second PFET when said signal at said output node is HIGH, and said signal at said feedback node transitions HIGH to turn OFF said second PFET when said signal at said output node is LOW.

7. (Previously Presented) The circuit as defined in claim 1 wherein, in operation, said first PFET is always ON, and a gate of said second PFET is connected to a feedback signal from said output node.

8. (Original) The circuit as defined in claim 7 wherein said second PFET is turned ON when a signal at said output node is HIGH, and turned OFF when said signal at said output node is LOW.

9. (Currently Amended) A ~~pseudo-NMOS~~logic circuit for reducing output noise, said circuit comprising:

a pseudo-NMOS circuit, said pseudo-NMOS circuit comprising:

a load PFET electrically connected between a power supply and an output node;

an NFET circuit having a plurality of inputs connected between said output node and ground for performing a predetermined function based on signals applied to said inputs and outputting a signal to said output node;

a feedback PFET electrically connected between said power supply and said output node for reducing noise at said output node based on said signal at said output node;

a feedback circuit electrically connected to said feedback PFET, wherein said feedback circuit sets said feedback PFET to ON when said signal at said output node is HIGH, and sets said feedback PFET to OFF when said signal at said output node is LOW.

10. (Cancelled)

11. (Previously Presented) The circuit as defined in claim 9 wherein an output of said feedback circuit is LOW when said signal at said output node is HIGH, and said output of said feedback circuit is HIGH when said signal at said output node is LOW.

12. (Previously Presented) A method for reducing noise at an output of a pseudo-NMOS circuit having a load PFET and an NFET function circuit, said method comprising the steps of:

providing a second PFET in parallel with the load PFET between a power source and the NFET function circuit; and,

turning said second PFET ON when said output of the pseudo-NMOS circuit is HIGH, and turning OFF said second PFET when said output of the pseudo-NMOS circuit is LOW.

13. (Original) The method as defined in claim 12, wherein said second PFET is turned ON and OFF by a feedback circuit connected to an output node of the pseudo-NMOS circuit.

14. (Original) The method as defined in claim 13, wherein said feedback circuit is an inverter circuit having an input connected to said output of the pseudo-NMOS circuit and an output connected to said second PFET.